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Document Title **Calorimeter Electronics System – Conceptual Design**		

Gamma-ray Large Area Space Telescope (GLAST)

Large Area Telescope (LAT)

Conceptual Design of the Calorimeter Electronics System

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CHANGE HISTORY LOG

Revision	Effective Date	Description of Changes

1 PURPOSE

This document describes the conceptual design for the GLAST Large Area Telescope (LAT) Calorimeter Electronics System.

2 SCOPE

This document gives an overview over the conceptual architecture of the GLAST LAT Calorimeter Electronics System.

3 DEFINITIONS

3.1 Acronyms

GLAST – Gamma-ray Large Area Space Telescope
GRB – Gamma-Ray Burst
LAT – Large Area Telescope
TBR – To Be Resolved
ACD – Anti-Coincidence Detector
TKR – Tracker Detector
CAL – Calorimeter Detector
TRG – L1 Trigger
GLB-TRG – Global L1 Trigger
TEM – Tower Electronics Module

3.2 Definitions

μsec, μs – Microsecond, 10^{-6} second
Dead Time – Time during which the instrument does not sense and/or record gamma ray events during normal operations.
s, sec – seconds
Simulation – To examine through model analysis or modeling techniques to verify conformance to specified requirements

4 APPLICABLE DOCUMENTS

Documents that are relevant to the development of the GLAST electronic system concept and its requirements include the following:

4.1 Requirement Documents

GE-00010, "GLAST LAT Performance Specification", August 2000
GLAST00010, "GLAST Science Requirements Document", P.Michelson and N.Gehrels, eds, July 9, 1999.
Add more

4.2 Conceptual Design Documents

[1] LAT Electronics System – Conceptual Design

[2] LAT Conceptual Design of the GLAST Calorimeter Front-End (GCFE) ASIC

[3] LAT Conceptual Design of the GLAST Calorimeter Readout Controller (GCRC) ASIC

[4] LAT TKR-CAL Tower Electronics Module – Conceptual Design

[6] LAT Control Protocol within LAT – Conceptual Design

[7] LAT Data Protocol within LAT – Conceptual Design

[8] LAT Housekeeping within LAT – Conceptual Design

[9] LAT L1 Trigger System – Conceptual Design

[10] LAT ACD-TRG Tower Electronics Module – Conceptual Design

[11] LAT TEM-Interface Card – Conceptual Design

5 INTRODUCTION

The *GLAST* electronics system comprises a number of front-end electronics subsystems i.e. TKR (Tracker), CAL (Calorimeter), ACD (Anti-Coincidence Detector), the TRG (Trigger), House-keeping (HSK), and the OEP (On-line

Event Processing) system. The overall architecture of the electronics system is described in [1]. This document outlines a conceptual design for the calorimeter systems electronics architecture and its control and dataflow interface with the TKR-CAL TEM (Tower Electronics Module).

Only one tower of the 16 towers in the LAT is described in this document. All 16 towers are identical as far as the calorimeter electronics is concerned.

6 ELECTRONICS ARCHITECTURE

IMPORTANT: CHANGE THE SIGNAL NAMES (Interfaces) TO MATCH THE System-wide AGREED-ON NAMES IN THIS DOC. All I/O names have to be agreed on by the Project Electronics Engineer.

6.1 TEM-Calorimeter Overview

Figure 1 shows a blockdiagram of the electronics system. There are 8 layers of 12 crystals to be readout. The 8 layers are divided in 4 x-layers and 4 y-layers. Each layer is readout from both ends of the crystals, herein called left and right. The front-end electronics is located on 4 AFEE (Analog Front-End Electronics) boards of the tower as illustrated in Figure 1. Each of the AFEE-boards serves one side of 48 crystals (= 4-layers x 12-crystals).

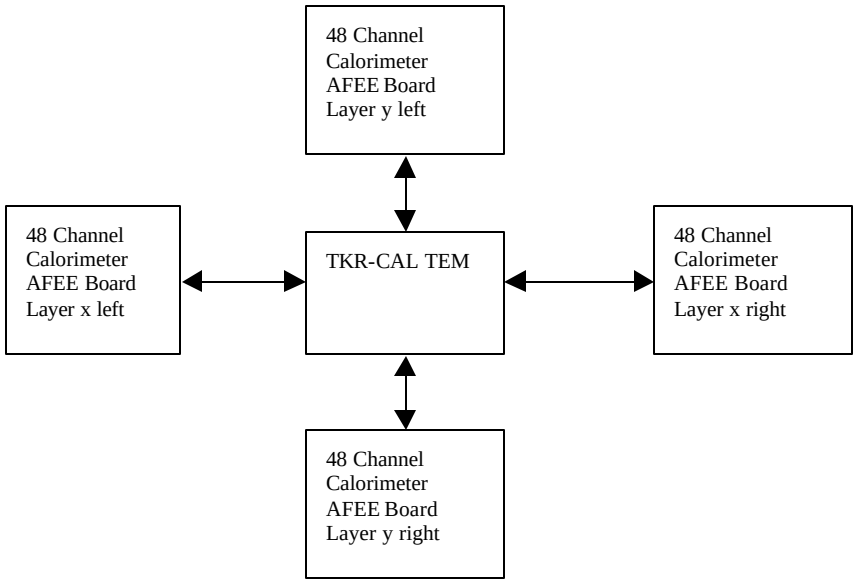

Figure 1: Organization of Calorimeter System on a TKR-CAL tower

Figure 2 shows one of the four 48-channel AFEE boards. It is organized in 4 layers of 12 signal channels with each layer controlled by a layer GLAST Calorimeter Readout Controller (GCRC) [2]. A GCRC controls 12 GLAST Calorimeter Front-End (GCFE) ASIC's [3]. A calibration DAC common to all channels on the AFEE-board is also shown in Figure 2. The board contains thus a total of 48 GCFE's, 4 GCRC's, 48 COTS ADC's and 1 COTS DAC (plus connectors, capacitors, and resistors).

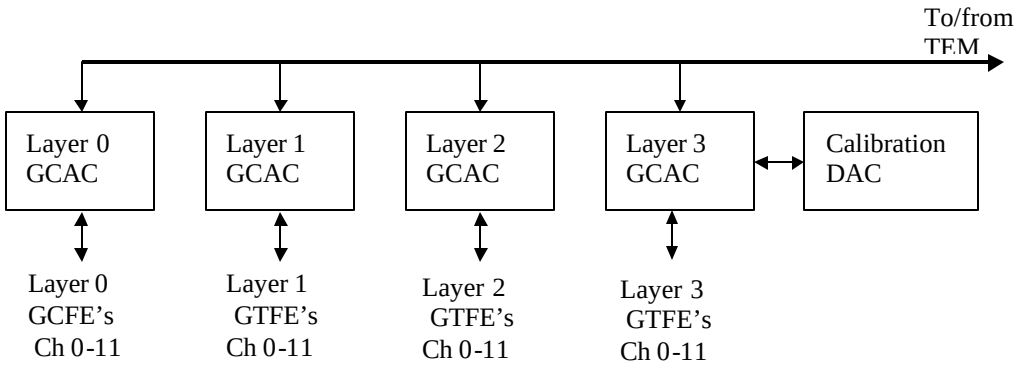

Figure 2: Organization of an AFEE-board

In Figure 3 one of the layers with its GCRC is shown in more detail. Each of the 12 GCFE's is communicating with the GCRC. The analog signal from the GCFE is digitized by an ADC and read out to the GCRC. Only the GCRC is communicating with the TEM.

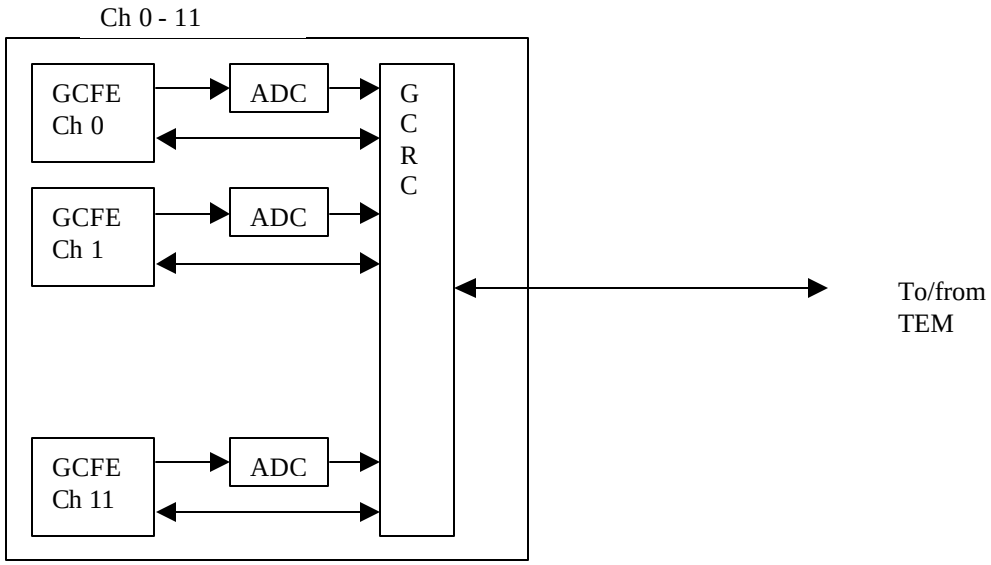

Figure 3: One Layer of the Calorimeter AFEE-board with its GCRC

6.2 Communication

6.2.1 Control and Setup

The GCRC receives control and setup commands from the TEM. The serial protocol consists of address, function, and data fields. The serial protocol is transported via a differential LVDS connection. An LVDS 20-MHz clock is supplied for timing. There are 14 bits in the address field, 5 bits in the function field, and a fixed number of bits in the data field, followed by a parity bit, all MSB first [4].

Figure 4 shows the interconnections for the commanding. The CMD, CLK, and RST lines are bussed to all 4 GCRC's. In order to prevent that one defective GCRC input can disable one AFEE board, the inputs are isolated via resistors. The address field from the TEM is used as follows: (In the Appendix the bits are defined)

- The first 6 address bits are not used in the calorimeter system and are stripped in the GCRC.
- The next 3 address bits determine which layer is being addressed, "111" is the broadcast address. (The GCRC has 2 hard-wired I/O bits to indicate its address, plus one I/O to indicate the end of the crystals, left or right.)
- The next bit determines whether the command is for the GCRC or any of its GCFE's.

If the command is for a GCFE, the GCRC forwards the remaining 4 address bits, 5 function bits, and data to all the GCFE's on its layer. If the command is for the GCRC, the remaining 4 address bits are ignored. The GCRC checks the parity bit (see Appendix for more details).

All GCFE's on a layer are bussed. Note that it is acceptable that one failing GCFE can disable the operation of one layer.

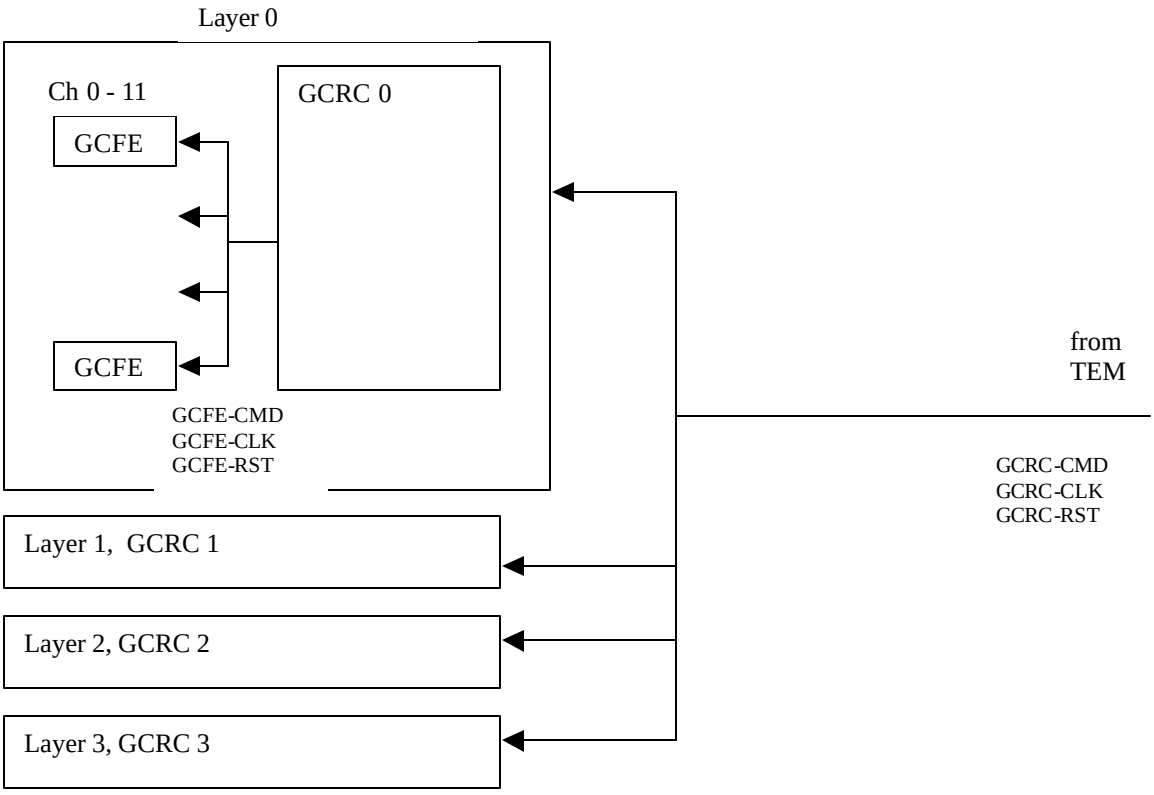

Figure 4: Control Path

The 4 GCFE address bits are decoded in the GCFE and are compared to its 4 hard-wired I/O pin levels indicating its location on the board. In order to have only one type of AFEE-board for the left and right side, a board common jumper indicates right or left orientation. This bit is used together with the 4 hard-wired I/O address pins to select the GCFE. The right side is addressed/readout from 0 to 11, the left from 11 to 0 (tbr), to synchronize the readout order of the log-ends from the board.

The command the GCFE's receive will be: Start-bit (added by GCRC), 4 address bits, 5 function bits, and 16 data bits. Parity between the GCRC and GCFE is not required since the communication is within a board.

The 5 function bits are decoded in the addressed component, GCRC or GCFE. Since each write command must have an associated read-back command, 16 different write/read functions can be used.

The calibration DAC, one per AFEE-board, is controlled by one of the GCRC's. There is only one design for all GCRC's for simplicity, which means that all GCRC's contain the logic and I/O's to decode and control a calibration DAC. However on the board only one of the GCRC's, layer 0 (tbr), is connected to the calibration DAC. (Alternatively one DAC per layer can be used if the power/space is small).

The bit rate for the transfer of commands from the TEM is 20 Mbps. A clock is distributed parallel to the command link to all GTRC's. The GCRC's are clocked continuously. The GCFE's are clocked from the GCRC only when needed (pulse-train).

Note that there is no automatic acknowledgment, e.g. echoing, resulting from the execution of a register write to the GCRC's and GCFE's. The verification of a write is by non-destructive read-back only, as described in the following section.

Write/Load commands can be broadcast via the addressing field to all AFEE boards, all layers, and/or all GCFE's. For the read commands however no broadcast is used, each register is read back individually.

6.2.2 Readback Data

Commands to read back registers are sent to the GCRC and GCFE (via the GCRC) as discussed in the Commanding section. The function code specifies a read function. The data field is 16-bit fixed, MSB first. If the useful data is less than 16 bits, the fill bits are sent first with the required bits following (check). The read must be non-destructive, which in general requires two latches for each bit. (The register content is copied to a read-register before shifting out).

The GCFE responds to a register read command with a start-bit followed by the data field. Each GCFE is connected with its own data line to its GCRC. However only one GCFE is addressed to read back data at any given time. (Each GCFE has its own data-line to the GCRC for the simultaneous transfer of data during signal acquisition, as well as for failure effects considerations.)

The data from the GCFE addressed is read out via the GCRC to the TEM. Each GCRC has its own dataline to the TEM, for layer separation. The GCRC starts the transmission with a start bit, followed by the data. A parity bit is appended at the end of the data-stream [3]. If the register to be read back is located in the GCRC, the transmission consists also of a start-bit, followed by the data field, followed by the parity bit.

(The baseline is that all registers in the GCRC are as well 16-bit wide. However, if it is required that the data-fields have to be 32-bit or longer (tbr), then the GCRC must insert a '1' after each set of 16-bit data to ensure that there are no 32 zero's (end of event trailer) in the data stream. In addition all data-fields from the GCRC to the TEM have to be equal, that means the readout field of the GCFE registers would have to be padded, in the GCRC, to the length of the GCRC registers. It is thus preferred to use 16-bit registers throughout the CAL AFEE system.)

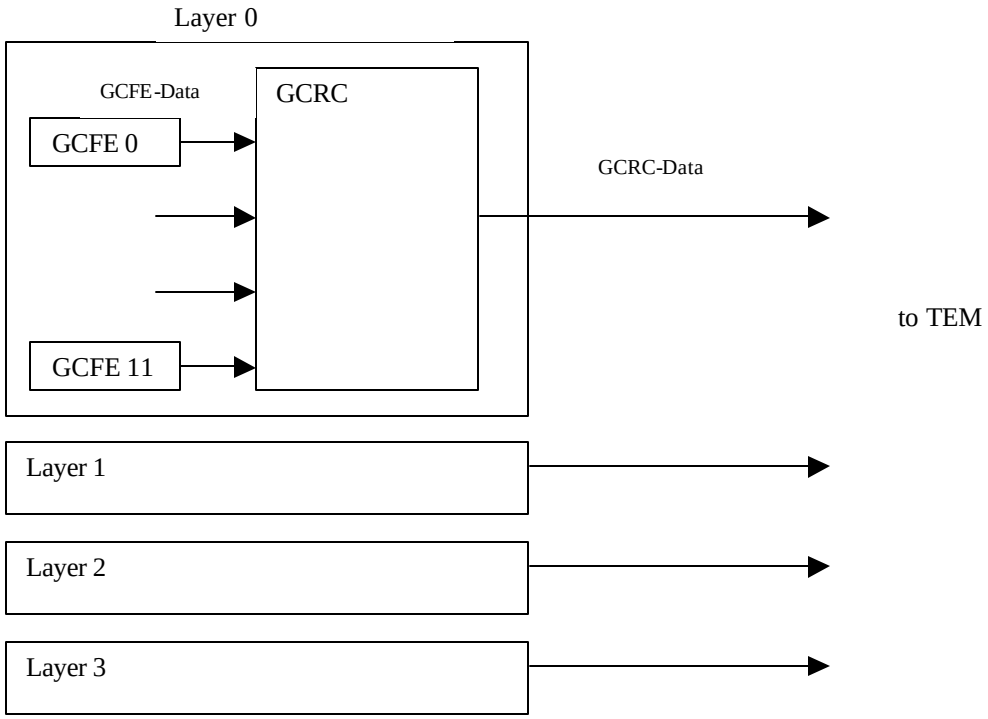

Figure 5: Readback Data Path

6.3 Trigger

6.3.1 Trigger Primitives to TEM

Each signal channel in the calorimeter contains two discriminators, LE-DISC and HE-DISC, which are used for making trigger decisions. Figure 6 shows the system for the trigger primitives. The LE-DISC and HE-DISC outputs of the 12 GCFE's on a layer are combined (wire-or), and connected to its GCRC. The GCRC outputs the combined signal to the TEM.

There are rate-counters counting the Layer-LE-DISC and Layer-HE-DISC's in the GCRC (tbr), for a total of 8 counters. The GCFE's do not contain any rate-counters to count each channel, but the GCFE LE-DISC and HE-DISC outputs can be enabled/disabled so that the hot channels can be tracked down via the layer counters.

Alternatively to the rate-counters being in the GCRC, there may be one rate-counter for each, HE-DISC and LE-DISC, signal on the TEM, which can be read out while the trigger is enabled.

In non-run mode the rate-counters are reset, started, stopped, and read out by commands. In run mode (for TEM counters), the rate-counters can be read out as part of the event. The trigger type received from the global trigger system indicates whether to attach the rate-counter states to the event or not.

Note to Neil: since it sure looks like an ASIC on the TEM for CAL/TKR/TRG control is way to go, putting the rate-counters in there is probably our best solution.

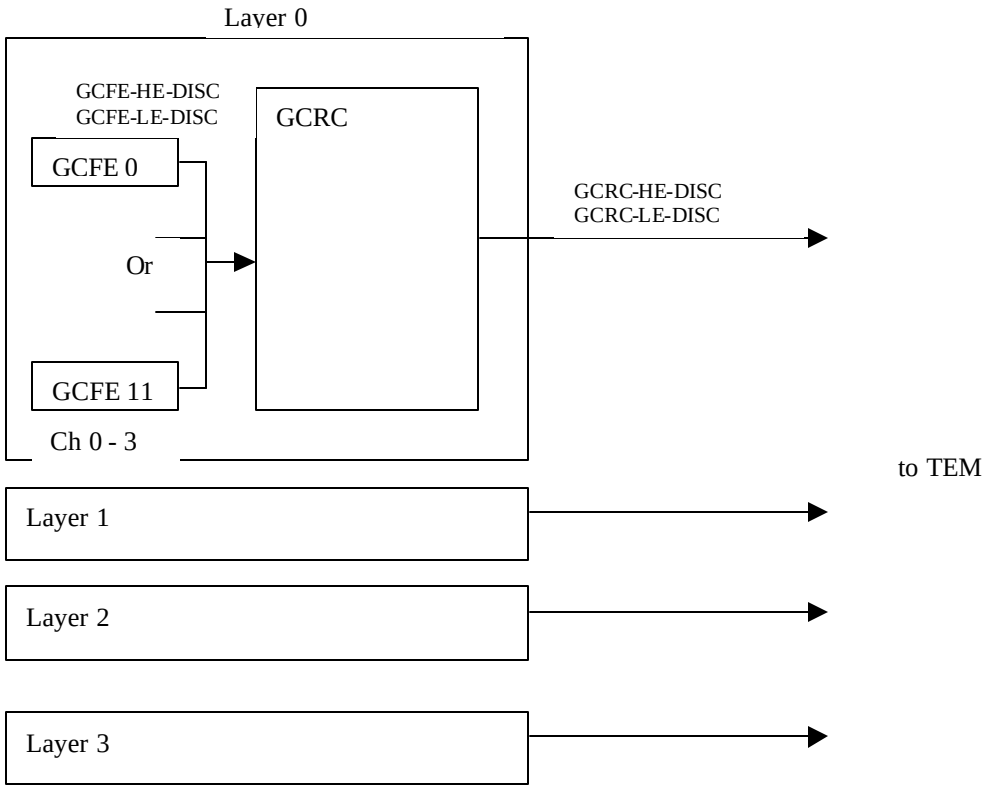

Figure 6: Trigger Primitives

6.3.2 Trigger Acknowledge Signal from TEM

The GLAST global trigger system generates an L1 trigger acknowledge signal which is delayed on the TEM and forwarded, called ACQ_START, to the AFEE-board as shown in Figure 7. The serial ACQ_START signal carries one additional bit, indicating whether to digitize all 4 ranges or only the auto-range selected (CNOM, Carbon-Nitrogen-Oxygen Mode bit). The GCRC forwards only the ACQ_START bit to the GCFE's. Subsequently the GCRC will generate a train of pulses on the clock line to the GCFE's and to the ADC's, which will result in the digitization and readout of the signals as described in the Event Data Readout section.

(Note: alternatively to the common delay of the trigger acknowledge signal on the TEM, it could also be delayed in each GCRC separately. This would only be needed if the wake-up function, available in some ADC's, were used. However the wake-up time of most ADC's is several times larger than can be compensated by an early notification, (at most 1 usec difference). It needs to be decided whether the power saving is worth the additional dead time. It also needs to be checked whether the earlier digital signal can still change the analog signal acquired. (Probably that is ok)

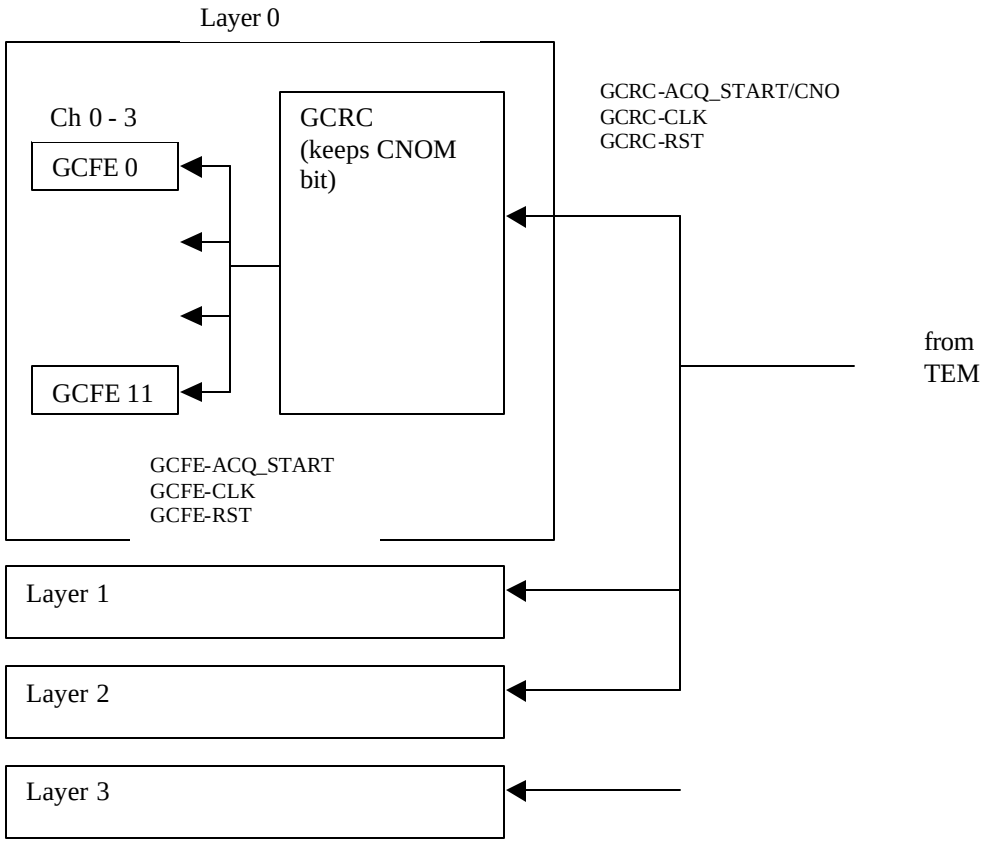

Figure 7: Start Acquisition Distribution

6.4 Event Data Readout

The GCRC receives the GCRC_ACQ_START signal with the CNO mode bit. The GCFE's receive the GCFE_ACQ_START signal from the GCRC.

The state-machines in the GCRC and GCFE cycle through their states with the 20-MHz system clock and the pulse-train generated by the GCRC, respectively.

The GCFE holds the analog signal on the first pulse and decides which range to connect to its analog output on the second pulse. Depending on the CNOM bit in the GCRC the GCRC state-machine controls the GCFE to either output one range or four ranges. The order of the ranges can be selected at configuration time via GCFE registers [2].

The GCFE sends the output of the log-accept discriminator bit and the range-bits to the GCRC via the data line controlled by pulses on the clock line originating in the GCRC state-machine. Figure 8 shows a diagram for the event data readout.

The GCRC state-machine generates signals to digitize and readout the 12 ADC's on a layer. The data is read into the GCRC and transferred to the TEM with a header and a trailing parity bit. There are two methods under discussion on how to handle this event data.

1. Multiplexing the ADC bits real-time from the ADC's to the TEM.
2. Storage of all ADC data in an event buffer in the GCRC with subsequent transmission to the TEM, zero-suppressed or not.

Note to Neil: I still have all the options in this doc to help my memory, However since we more likely than not have an ASIC on the TEM, I think the cleanest solution is 1.

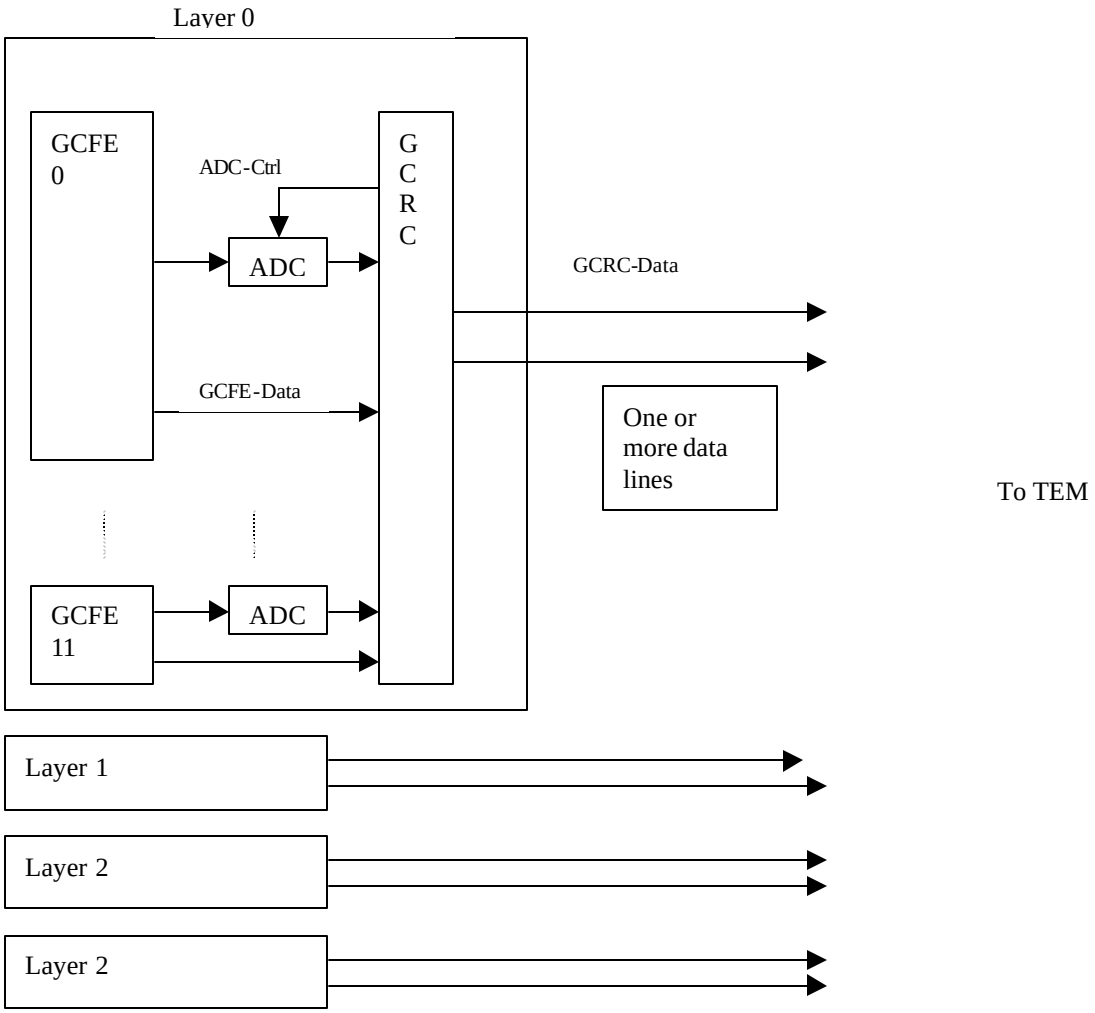

Figure 8: Event Readout

6.4.1 Option without event buffer in GCRC

The serial data from the ADC's are multiplexed real-time onto the data line to the TEM. This method optimizes the time of the transmission from the ADC's to the TEM. The data is entirely on the TEM a few clock-cycles after the last ADC bit is available. The advantage of the method is that the data transmission from the GCRC to the TEM can occur while the trigger system is still disabled without impacting the total dead-time considerably. This is only important if the transmission from the GCTC to the TEM interfers with the trigger system, i.e. leads to self-triggering of the calorimeter by crosstalk from the digital data-lines to the amplifier inputs. Another advantage is that the TEM does not need to queue time and event stamps for interleaved triggers for the CAL (check). The main disadvantage is that the channel data arrives bit-interleaved at the TEM, requiring a bit-serial-in register for each channel assuming that the data in the memory is to be organized in channels. In real terms this requires a custom digital ASIC on the TEM. (If for other reasons there is an ASIC on the TEM, then this disadvantage disappears).

The data readout is preceeded by an header (may only be a start bit, tbr) and a parity bit as appended at the end. The TEM state-machine knows whether a single-range or four-range read out is under way and transfers the data into TEM memory accordingly. No event trailer is needed for the transfer of data from the AFEE to the TEM.

6.4.2 Option with Event buffer in GCRC

The serial data output from the ADC's (12 bits for each ADC) are stored completely into a GCRC event buffer before transmission to the TEM. This enables the transmission of the 13-bits per channel (1 log-accept bit, 2 range-bits, and 12 ADC bits) from the GCRC, channel by channel, MSB first. This simplifies the TEM electronics since it can

implement a serial-to-parallel conversion with one register per data-line and subsequent storage in a word-organized memory (e.g. 16-bit wide memory). This method requires the transmission of event data from the GCRC to the TEM while the trigger is active in order to meet the dead-time specification (check). In CNO mode the data of a range is transferred to the TEM while the ADC bits from the next range are transferred from the ADC to the GCRC.

The data may or may not be zero-suppressed in the GCRC. Again, if the logic on the TEM is in an ASIC, then the zero-suppression on the TEM may be preferable.

6.5 Event Data Readout Time

6.5.1 Option without event buffer in GCRC

The analog GCFE signal is held 3.5 usec after the event time. The first range should be settled 2 usec after and digitiation can commence. The digitization time of the e.g. MAX1240 is 7.5 usec. The minumum readout time from the ADC to the GCRC at 2 MHz is 6.5 usec (13 clock cycles to read out 12 bits). If the 12 ADC outputs are multiplexed to a single data line to the TEM, then the maximum frequency to readout the ADC's is 20 MHz divided by 12 = 1.67 MHz. The ADC readout time is thus 7.8 usec. That means that there could be new ADC data every 15.3 usec. However if one assumes that there is feedthrough from the ADC output to the GCFE input while data is transferred from the ADC to the GCRC, then one has to wait at least

- For the trigger: > twice (tbr) the trigger shaping time of 500 ns after the transfer of the last ADC bit before the trigger can be reenabled. That results in time of first trigger + 3.5 usec + 2 usec + 7.5 usec + 7.8 usec + 1 usec = 21.8 usec between acquisitions.
- For the data: instead of twice (tbr) the fast shaping time one has to wait at least twice (tbr) the long 3.5 usec shaping time which would result in a total of 27.8 usec deadtime.

The last data bit is transferred from the GCRC to the TEM twelve 20-MHz clock cycles after the last ADC bits are available, or 0.6 usec.

In four-range readout the wait time due to the feedthrough to the amplifier input only needs to be observed for the last range readout. The total deadtime is thus first trigger + 3.5 usec + 4 x (2 usec + 7.5 usec + 7.8 usec) + 1 usec = 74 usec between acquisitions for the trigger. For the data the deadtime is an additional 6 usec. Note that a second data pipe from the GCRC to the TEM can only reduce the deadtime by 1.3 usec if the maximum ADC readout frequency is 2 MHz.

If the ADC could be read out at a frequency of at least 3.3 MHz, then two data pipes from the GCRC to the TEM could reduce the deadtime to first trigger + 3.5 usec + 2 usec + 7.5 usec + 4 usec + 1 usec = 18 usec between acquisitions (plus 6 usec for data).

If the wake-up function of one of the ADC's is used, then the above dead-time needs to be increased.

Note that these times change considerably if a faster ADC e.g. 1MSPS-AD7475 is used.

6.5.2 Option with Event buffer in GCRC

The ADC data is buffered in the GCRC and then readout to the GCRC at a rate of 20 Mbps. The data from the ADC can be transferred to the GCRC at the maximum ADC readout frequency. The readout time from the GCRC to the TEM on a single pipe per layer is 12 channels x 15 bits = 180 bits or 9 usec. Assuming that the trigger system can be enabled while the data is transferred from the GCRC to the TEM, the dead time is first trigger + 3.5 usec + 2 usec + 7.5 usec + 6.5 usec + 1 usec = 20.5 usec between acquisitions (plus 6 usec if the feedthru to the analog data is taken into account). Note that the transfer time of the data from the GCRC to the TEM in single range readout is less than 3.5 usec + 2 usec + 7.5 usec which means that the event buffer in the GCRC is empty before new ADC data is generated and does thus not impose additional dead-time.

If the trigger system is disabled while dta is transferred to the TEM, then more pipe to transfer the data from the GCRC to the TEM may be required for keep the dead-time as required. However this increases the power dissipation (lvds links) as well as the number of TEM FPGA/ASIC pins and logic required.

In CNO mode (readout of 4 ranges) there may be a longer readout time (approximately 3 x 1.5 usec = 4.5 usec longer) if one pipe per layer is used unless the buffer in the GCRC is implemented as a FIFO. (Since the CNO is not frequent the longer deadtime for a single data pipe seems acceptable).

The GCRC contains four (because of all range readout) sets of 12 registers (12 channels per layer) to hold the 12-bit data, 2-bit range, and 1 bit zero-suppress information from the 12 channels on one layer.

In auto-range mode, the GCRC applies a reset signal to the GCFE's as soon as the ADC data is transferred to the GCRC. This will put their state-machines into idle state and a new trigger may thus occur.
Subsequently the registers from the layer-GCRC are read to the TEM at a rate of 20 Msps. The state-machine on the GCRC cycles through the 12 channels on its layer and, depending on the log-accept list, skips over channels to be suppressed. The log-accept list is generated from its own log-accepet bits and the 48 log-accept bits received via the TEM from the opposite log ends (needs more explanation, note that this requires that the log-accept bits are transmitted to the opposite AFEE before zero-suppression, and that a mask is used in addition to overwrite failing logs).
The transfer time of ADC data to the TEM is from ~0 (no channels readout) to x usec (all 12 channels readout). Here it is assumed that each channel carries 2 range bits, 12 ADC bits, 4 log ID bits and a framing bit (not necessarily required, but simplifies control on the TEM?).

6.5.3 TEM Data-Format

To follow.

6.6 House-Keeping

Only a few environmental sensor are to be readout from the AFEE-boards. Environmental sensors are handled as part of the TEM house-keeping [2, 4]. (List the signals here). There are also low-rate science (LRS) counters as follows

- tbr

6.7 Clocking

The GCRC is continously clocked at 20 MHz (not absolutely required but simpler, tbr).
The clock line (or better timing line) to the GCFE carries a stream of pulses generated in the GCRC with a maximum frequency of 20 MHz.

6.8 Calibration

The GCRC's receives a calibration strobe command from the TEM. It generates a differential calibration strobe which is connected to each GCFE. The calibration strobe is thus not a command routed to the GCFE's to reduce digital cross-talk.
In order to generate a L1 trigger acknowledge (L1TACK) one can either

- let a channel generate a LE-DISC via its discriminator which then will lead to a L1TACK from the global trigger system, or
- let the TEM generate a Layer-LE-DISC (probably preferred).

There are no minor (# of strobes) or major (# of DAC values) loops within a sub-system to acquire calibration data. The calibration strobe is originated (one by one) at a higher system level. The TEM receives the calibration command, generates a trigger signal request (tbr) to the global trigger, which issues a L1TACK. In order to be able to scan the analog GCFE waveform for diagostics reasons, the calibration strobe issued to the AFEE can be delayed via a programmable TEM register (or is L1TACK delay programmability sufficent?)

6.9 TEM Electronics

- (This section needs work, detail in [2]).

7 GCFE Function Allocation and Interconnections

Figure 9 (not yet) shows the GCFE with its I/O's. (Names arbitrary and subject to change). Power ppins are omitted.
(d) means differential, (s) single-ended, (d/s) not clear if s or d.
List of I/Os: (see figure in the doc for clarification)

7.1 GCFE Function

Analog processing
Sample-and-hold's
Range-selection
Trigger circuitry

State-machine for configuration and readback
State-machine for acquisition of data (started by ACQ_START, advanced by pulse-train, reset to stop/reset)

7.2 Pins

7.2.1 Inputs:

2 x Analog-In (s)
Calibration-Strobe (d)
Calibration-Voltage (d)
GCFE-Reset (d)
GCFE-ACQ_START (d) (delayed trigger acknowledge signal bit)
GCFE-CLK (d) (stream of pulses, should be globally renamed to Timing signal)
GCFE-CMD (d) (could be single ended since only used in configuration, but rate-counters? tbr)
4 x GCFE-Address (s), addresses one or all of 12 channels on a layer, note that layer is addressed from GCRC
1 x left/right AFEE board bit

7.2.2 Outputs:

GCFE-LE-DISC (d)
GCFE-HE-DISC (d)
GCFE-Data (d) carries read-back data, ZS-bit, and range-bits, depending on when in cycle.
GCFE-Analog-out (s), analog signal to ADC

7.2.3 Pin-Count

Total: 24 pins, plus some analog bias pins, plus external shaper pins, plus power
Use 44-pin TQFP.

7.2.4 Note

If 2 channel GCFE, then add 2 x analog-in, 1 x Analog out, 6 external shaper pins, additional power pins. Use 64-pin PQFP.

8 GCRC I/O, one per 12 logs, including all buffering

This describes the GCRC serving an entire layer, including buffering of signals to/from TEM.

8.1.1 Inputs

From TEM: (10 pins)
GCRC-Reset (d)
GCRC-LITACK (d)
GCRC-CLk (d)
GCRC-CMD (d)
CAL-Strobe (d)

From GCFE: (28 pins)
GCFE-LE-DISC (d), OR of all GCFE
GCFE-HE-DISC (d), OR of all GCFE
12 GCFE-Data (d), one from each GCFE NOTE: this line could be reduced by e.g. using enables (12 single ended pins plus 1 Data (d) = 14 pins, saving of 10 pins. But then have range-bit readout during digitization, problem?). No decoding used because no additional GCFE pins are available.

Other: (16 pins)
12 x ADC-data
2 x GCRC-Address (s)
1 x left/right address? check

8.1.2 Outputs

To TEM: (6 pins with N=1)
GCRC-LE-DISC (d)
GCRC-HE-DISC (d)
N x GCRC-Data (d) carries read-back and event data

To GCFE: (10 pins)
GCFE-Reset (d)
GCFE-ACQ_START (d)
GCFE-CLk (d)
GCFE-CMD (d)
Cal-strobe (d)

Other: (9 pins)
ADC-control (s), 3 (tbr) signals bussed to all 12 ADC's
CAL-DAC control (s), 3 (tbr)
1 x Power
1 x Ground
1 x Driver current set

8.1.3 Pin-Count:

Total: 78 pins. Use 80 TQFP

9 GCRC I/O, one per 12 logs, all buffering in a separate buffer

This describes the GCRC serving an entire layer, but all buffering is done in an external LVDS driver. More power, more components.

9.1.1 Inputs

From TEM: (8 pins)
GCRC-Reset (d)
GCRC-LITACK (d)
GCRC-CLk (d)
GCRC-CMD (d)

From GCFE: (24 pins)
12 GCFE-Data (d), one from each GCFE. NOTE: this line could be reduced by e.g. using enables (12 single ended pins plus 1 Data (d) = 14 pins, saving of 10 pins. But then have range-bit readout during digitization, problem?). No decoding used because no additional GCFE pins are available

Other: (15 pins)
12 x ADC-data
2 x GCRC-Address (s)
1 x left/right address? check

9.1.2 Outputs

To TEM: (2 pins with N=1)
N x GCRC-Data (d) carries read-back and event data

To GCFE: (8 pins)
GCFE-Reset (d)
GCFE-ACQ_START (d)
GCFE-CLk (d)
GCFE-CMD (d)

Other: (9 pins)
ADC-control (s), 3 (tbr) signals bussed to all 12 ADC's
DAC control (3 pins, tbr)
1 x Power
1 x Ground
1 x Driver current set

9.1.3 Pin-Count:

Total: 66 pins. Still use 80 TQFP.

- *Elimination of DAC control would make it fit in 64 TQFP, but then TEM has to write/read DAC.*
- *Reduction by above 10 Data pins and driver current pin would make it fit in 52 pin QFP.*

10 GCRC I/O, one per 4 logs, all buffering and DAC external

This describes the GCRC serving 4 logs. DAC needs to be controlled by TEM, also need external LVDS drivers. More power but how much..

10.1.1 Inputs

From TEM: (8 pins)
GCRC-Reset (d)
GCRC-LITACK (d)
GCRC-CLk (d)
GCRC-CMD (d)

From GCFE: (8 pins)
4 GCFE-Data (d), one from each GCFE. Could be reduced to 5, 4 single-ended select plus 1 differential Data.

Other: (9 pins)
4 x ADC-data
4 x GCRC-Address (s), addresses one or all of 4 layers
1 x left/right address? check

10.1.2 Outputs

To TEM: (2 pins with N=1)
N x GCRC-Data (d) carries read-back and event data

To GCFE: (8 pins)
GCFE-Reset (d)
GCFE-ACQ_START (d)
GCFE-CLk (d)
GCFE-CMD (d)

Other: (6 pins)
ADC-control (s), 3 (tbr) signals bussed to all 12 ADC's
1 x Power
1 x Ground
1 x Driver current set

10.1.3 Pin-Count:

Total: 41 pins. Use 44 TQFP. Can't fir in 32-TQFP.

11 GCRC preliminary conclusion

- Best is 80-TQFP, if there is space
- Next is 64-TQFP but: TEM DAC control which requires more cables plus LVDS conversion of 3 signals (2 IN, 1 OUT). Plus need LVDS buffers for CALStrobe and HE-DISC, LE-DISC
- Next is 52-TQFP which requires that Data-out lines from GCFE are tri-state plus risk of cross-talk from range-bits to other ADC acquisitions.
- Next is 44-TQFP but then need three for each layer. Does not seem good choice to trade one 52 or 64-pin device per layer for three 44-pin devices.

12 Cable to TEM

The cable from the AFEE-board to the TEM has power plus:

12.1.1 Input

1 x CMD (d), bussed to all GCRC
1 x CLK (d), bussed to all GCRC
1 x RST (d), bussed to all GCRC
1 x LITACK (d), bussed to all GCRC

12.1.2 Output

4 x LE-DISC (d), one per layer
4 x HE-DISC (d), one per layer
N x Dataout (d)

Plus DAC control if required.

How about redundancy of cables? Maybe not required.